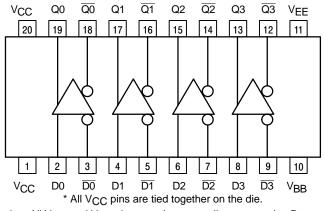
5V ECL Quad Differential Receiver

The MC100EL17 is a low-voltage, quad differential receiver. The device is functionally equivalent to the E116 device

Under open input conditions, the \overline{D} input will be biased at V_{CC}/2 and the D input will be pulled down to V_{EE}. This operation will force the Q output LOW and ensure stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 325 ps Propagation Delay
- ESD Protection: > 2 KV HBM, > 100 V MM
- The 100 series contains temperature compensation
- PECL Mode Operating Range: $V_{CC} = 4.2 \text{ V}$ to 5.7 V with $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -4.2$ V to -5.7 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at $V_{\mbox{\scriptsize EE}}$
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1 For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 141 devices



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Logic Diagram and Pinout: 20-Lead SOIC (Top View)

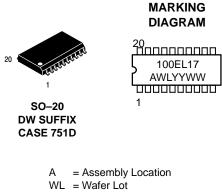
PIN DESCRIPTION

Pins	Function
Dn, Dn	ECL Differential Data Inputs
Qn, Qn	ECL Differential Data Outputs
V _{BB}	Reference Voltage Output
Vcc	Positive Supply
VEE	Negative Supply



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YY = Year

WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100EL17DW	SO-20	38 Units/Rail
MC100EL17DWR2	SO-20	1000 Units/Reel

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
VCC	PECL Mode Power Supply	V _{EE} = 0 V		8	V
VEE	NECL Mode Power Supply	ACC = 0 A		-8	V
VI	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	$\begin{array}{c} V_I \leq V_{CC} \\ V_I \geq V_{EE} \end{array}$	6 6	V
lout	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θJA	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θJC	Thermal Resistance (Junction-to-Case)	std bd	20 SOIC	30 to 35	°C/W
T _{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100EL SERIES PECL DC CHARACTERISTICS V_{CC} = 5.0 V; V_{FF} = 0.0 V (Note 2)

			–40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
IEE	Power Supply Current		26	31		26	31		27	33	mA
VOH	Output HIGH Voltage (Note 3)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
VOL	Output LOW Voltage (Note 3)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
VIH	Input HIGH Voltage (Single–Ended)	3835		4120	3835		4120	3835		4120	mV
VIL	Input LOW Voltage (Single–Ended)	3190		3525	3190		3525	3190		3525	mV
V _{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
VIHCMR	Common Mode Range (Differential) (Note 4) Vpp < 500 mV	1.3 1.5		4.6 4.6	1.2 1.4		4.6 4.6	1.2 1.4		4.6 4.6	V
Iн	Input HIGH Current			150			150			150	μΑ
۱ _{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / -0.5 V.
Outputs are terminated through a 50 Ω resistor to V_{CC} - 2.0 V.
V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between Vppmin and 1 V.

		–40°C			25°C						
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
IEE	Power Supply Current		26	31		26	31		27	33	mA
VOH	Output HIGH Voltage (Note 6)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
VOL	Output LOW Voltage (Note 6)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
VIH	Input HIGH Voltage (Single–Ended)	-1165		-880	-1165		-880	-1165		-880	mV
VIL	Input LOW Voltage (Single–Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
VBB	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
VIHCMR	$\begin{array}{llllllllllllllllllllllllllllllllllll$	-3.7 -3.5		0.4 0.4	-3.8 -3.6		0.4 0.4	-3.8 -3.6		-0.4 -0.4	V
Iн	Input HIGH Current			150			150			150	μΑ
IIL	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / -0.5 V.
 Outputs are terminated through a 50 Ω resistor to V_{CC} - 2.0 V.
 V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between Vppmin and 1 V.

MC100EL17

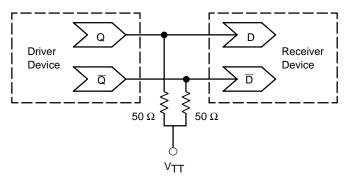
			–40°C 25°C								
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
fMAX	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
^t PLH ^t PHL	Propagation Delay Diff D to Q S.E.	330 280		530 580	350 300		550 600	360 310		560 610	ps
^t SKEW	Skew Output-to-Output (Note 9) Part-to-Part (Diff) (Note 9) Duty Cycle (Diff) (Note 10)			75 200 25			75 200 25			75 200 25	ps
^t JITTER	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
VPP	Input Swing (Note 11)	150		1000	150		1000	150		1000	mV
t _r t _f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

8. VEE can vary +0.8 V / -0.5 V.

9. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.

10. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.

11. Vpp(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.



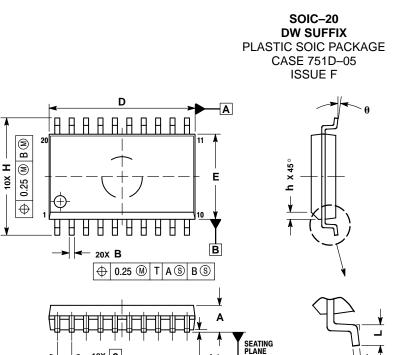
 $V_{TT} = V_{CC} - 2.0 V$

Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

- AN1404 ECLinPS Circuit Performance at Non–Standard VIH Levels
- AN1405 ECL Clock Distribution Techniques
- AN1406 _ Designing with PECL (ECL at +5.0 V)
- AN1503 ECLinPS I/O SPICE Modeling Kit
- AN1504 Metastability and the ECLinPS Family
- AN1560 Low Voltage ECLinPS SPICE Modeling Kit
- AN1568 Interfacing Between LVDS and ECL
- AN1596 ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650 _ Using Wire–OR Ties in ECLinPS Designs
- AN1672 The ECL Translator Guide
- AND8001 Odd Number Counters Design
- AND8002 Marking and Date Codes
- AND8020 Termination of ECL Logic Devices

PACKAGE DIMENSIONS



NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS. 2. INTERPRET DIMENSIONS
- INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M. 1994. DIMENSIONS D AND E DO NOT INCLUDE MOLD
- PROTRUSION
- MAXIMUM MOLD PROTRUSION 0.15 PER SIDE. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL
- BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS									
DIM	MIN	MAX								
Α	2.35	2.65								
A1	0.10	0.25								
В	0.35	0.49								
С	0.23	0.32								
D	12.65	12.95								
Е	7.40	7.60								
e	1.27	BSC								
Н	10.05	10.55								
h	0.25	0.75								
L	0.50	0.90								
θ	0 °	7 °								

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